Power Delivery Network Benchmarking for Interposer and Bridge-Chip-Based 2.5-D Integration

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***Abstract*— In this letter, a power delivery network (PDN) modeling framework for emerging heterogeneous 2.5-D integration platforms is presented. The framework is validated using IBM power grid benchmarks, and maximum relative errors of less than 7.29% and 0.67% for IR-drop and transient noise are shown, respectively. Next, the framework is used to evaluate interposer and bridge-chip-based 2.5-D integration platforms. The simulation results show that an interposer with dense power/ground grids and microbumps can suppress power supply noise (PSN) by a small margin. In bridge-chip-based 2.5-D integration, under the assumption that the bridge-chips underneath the active dice block direct access to package power/ground planes, some PDN considerations are highlighted and evaluated. Using multiple bridge-chips and smaller overlap areas between the bridge-chips and the active dice, the worst case PSN in bridge-chip-based 2.5-D integration is minimally impacted.**

***Index Terms*— di/dt noise, IR-drop, power delivery networks, interposer and bridge-chip 2.5-D ICs.**

I. Introduction

THE trends of lower supply voltage, higher current demand and increased power density are causing power delivery in high-performance digital systems to be an increasingly difficult challenge [1]. Moreover, there is an increasing need for heterogeneous integration of multiple dice of various functionality into a single package, which exacerbates the power delivery challenges. Power delivery network (PDN) and power supply noise (PSN) in traditional single-chip and 3-D ICs have been extensively studied in the literature [2]–[4]. However, 2.5-D integrated electronics have not been investigated as thoroughly. Specifically, 2.5-D ICs have several unique attributes that require consideration. For example, in a silicon interposer based 2.5-D integration [5], the use of power/ground (P/G) TSVs increases PDN parasitics. Likewise, for Embedded Multi-die Interconnect Bridge (EMIB) [6] and Heterogeneous Interconnect Stitching Technology (HIST) [7], signal interconnections and driver circuits are placed, generally, on the edges of the dice and above the bridge-chips, which may possibly lead to a reduction in the power/ground C4 bumps that have direct access to the package-level power/ground planes at the periphery. Therefore, in this letter, based on prior PDN modeling efforts for 3-D ICs [3], [8], we propose a PDN modeling framework to evaluate 2.5-D integrated systems. Moreover, the PDN of 2.5-D integrated electronics (interposer and bridge-chip based interconnections) is evaluated to explore challenges and opportunities in 2.5-D ICs.

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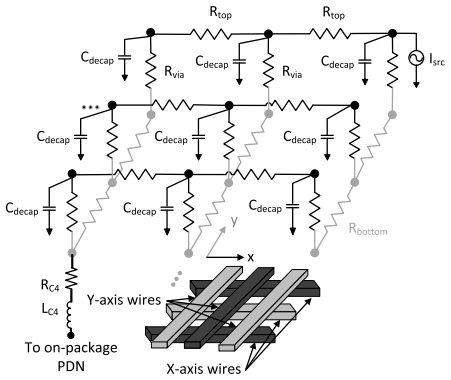


Fig. 1. Simplified on-die PDN model.

II. Modeling Methodology and Validation

In this work, we assume an ideal Voltage Regulator Module (VRM) supplying a stable voltage and use a lumped resistor/inductor network to model the board-level current spreading. A distributed package-level PDN model is implemented to reflect the spreading effects of current in the package. The package power/ground planes are modeled as two layers (i.e. two power and two ground layers), where the bottom layer is connected to the motherboard using BGAs, and the top layer is connected to the on-die PDN using C4 bumps. Each node in the two layers is connected to six adjacent nodes using a resistor-inductor pair either due to the package traces or inter-layer vias.

On-die PDN consists of several metal layers, where the power/ground wires are parallel to each other in each layer, but each layer is orthogonal to the layer below/above it (interleaved structure, as shown in the inset of Fig. 1). Prior work has proposed a virtual PDN mesh design using C4 bump granularity with only one metal layer [1], [2], [9]. However, to better reflect the nature of the interleaved PDN design as well as the impact of on-die vias, we model the on-die PDN as a two-layer structure, as shown in Fig. 1. For each layer,

TABLE I
VALIDATION RESULTS

case (# Nodes)	Max Bump Current Error (%)	Max IR Drop Error (%)	Max Transient Error (%VDD)
Ibm1 (31 K)	21.75	20.29	1.84
Ibm2 (127 K)	7.14	11.11	0.67
Ibm3 (852 K)	3.59	2.21	0.54
Ibm4 (954 K)	7.60	0.71	0.12
Ibm5 (1.08 M)	6.12	3.03	0.22
Ibm6 (1.67 M)	7.29	1.23	0.22
Ibm7 (1.46 M)	5.34	5.71	N/A
Ibm8 (1.46 M)	5.34	5.71	N/A

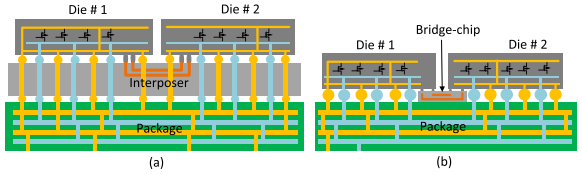


Fig. 2. 2.5-D integration platforms (a) interposer (b) HIST [7].

we map the fine-granularity PDN layout to coarse mesh grids using the model described in [9]. Lastly, all PDN layers with X-axis metal wires are mapped onto the top coarse layer, while the Y-axis metal wires are mapped onto the bottom coarse layer, as shown in Fig. 1.

We use the *IBM* power grid benchmarks [10] to validate the framework. The results are summarized in Table I. For steady-state analysis, except for the first two small cases, all cases obtain maximum relative errors of less than 7.60% and 5.71% in bump current and IR-drop, respectively. In the case of the transient results, we normalize the error to supply voltage because some of the benchmark noise values are small and thus, the relative error can be high. Except for IBM1, the maximum error for all cases is less than 0.67% VDD.

III. PDN EVALUATION OF 2.5-D INTEGRATION

Fig. 2 shows two 2.5-D integration technologies with different approaches for chip-to-chip interconnection. The first approach utilizes silicon interposer technology. In our study, we assume that the interposer contains a high-density PDN (i.e., grids) and that fine-pitch microbumps are uniformly distributed between each active die and the interposer-level PDN [11]. Moreover, we assume fine-pitch TSVs in the interposer are used to connect the interposer-PDN to the landing pads of the C4 bumps. Through the above PDN resources, the current has improved spreading due to the high-density microbumps and the additional interposer PDN.

The second approach, HIST [7], is based on placing 'stitch' chips above the package substrate between the active dice to route high-density chip-to-chip interconnects. Another approach is EMIB technology as described in [6], which utilizes embedded silicon chips within the package to route the chip-to-chip interconnects. Moreover, bridge-chips are used in the electrical and photonic macrochip approach [12]. For HIST, if no vias are used to penetrate the stitch-chips, this may limit the number of power/ground bumps that have direct access to the package-level power/ground planes in the periphery of the active dice. As a consequence, the PSN in those regions may be impacted, especially for large overlap areas between the stitch-chips and the active dice. In this letter, we assume that all chip bridging integration architectures provide no direct access between the on-die PDN and the package-level PDN in the periphery where the bridge-chips are located (and overlap). Under such an assumption, our results suggest

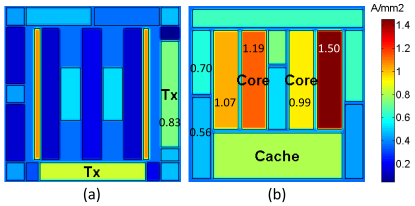


Fig. 3. The current density of each die. (a) Die #1 (b) Die #2.

TABLE II
PARAMETERS FOR PDN MODEL

Parameter	value
On-die global wire **P**itch/**W**idth/**T**hickness (μm)	39.5/17.5/7
On-die intermediate wire P/W/T (nm)	560/280/506
On-die local wire P/W/T (nm)	160/80/144
on-die decap density (nF/mm^2)	3.35
microbump pitch/R/L ($\mu m/m\Omega$/pH)	40/50.9/11.1
C4 bump pitch/R/L ($\mu m/m\Omega$/pH)	200/14.3/36.9
Package effective decap R/L/C ($(m\Omega$/pH/μF)	541.5/220.7/52
Package resistivity/inductance ($m\Omega/mm$/pH/mm)	1.2/24
BGA pitch/R/L ($\mu m/m\Omega$/pH)	500/38/46
bundled TSV pitch/R/L ($\mu m/m\Omega$/pH)	200/1.9/2.5
PCB R/L ($\mu\Omega$/pH)	166/21
PCB Decap R/L/C (($\mu\Omega$/nH/μF)	166/19.54/240

that the PDN model of HIST is relatively comparable to other 2.5-D bridge-based integration architectures, and thus, we refer to its results as 'bridge-chip' for the rest of the letter.

A. Design Parameter and Specification

In this study, we emulate a field-programmable gate array (FPGA)-processor 2.5-D integrated package. In our two-die package, Die #1 emulates a 14 nm FPGA die and is assumed to have a peak total current of 49.78 A [13], [14]. The emulated FPGA layout is based on *Intel* Stratix 10 FPGA [15]. Die #2 emulates a 22 nm processor with a peak total current of 82.77 A [16]. The current density maps are shown in Fig. 3. The supply voltage is assumed to be 0.9 V [14], [17]. Both dice are assumed to be 1 cm $\times$ 1 cm, and the package is assumed to be 2.45 cm $\times$ 1.8 cm. The two dice are placed side-by-side with a die spacing of 0.5 mm. Table II summarizes the parameters used in the PDN simulations.

Moreover, as a reference to the best achievable results for bridge-chip and interposer cases, we consider an ideal baseline case where the two dice are assumed to be bonded to the package without an interposer or bridge chips. This baseline is referred to as 'standalone' case. For all cases, we assume the packages are the same and utilize a C4 bump pitch of 200 μm. For the interposer case, the microbump pitch is 40 μm.

B. Benchmarking

1) IR Drop: IR-drop results are summarized in Fig. 4. With the addition of a dense P/G grid in the interposer, the IR-drop of the interposer case is 2.3% and 4.1% smaller than the standalone case for each chip, respectively. This is because the fine-pitch P/G grid and microbumps cause the current to spread more uniformly. Of course, the results are dependent on C4 bump and microbump pitches. If the C4 bumps become relatively denser in the standalone case, the modest benefits of interposer may decrease. Moreover, interposer technology may have higher fabrication costs, signal integrity issues for high speed ICs and mechanical reliability challenges [6]. For the bridge-chip case, compared to the standalone case, the additional noise is mainly due to the absence of C4 bumps in the regions overlapping with the bridge-chips. Therefore, the overlap areas between the bridge-chips and the active dice

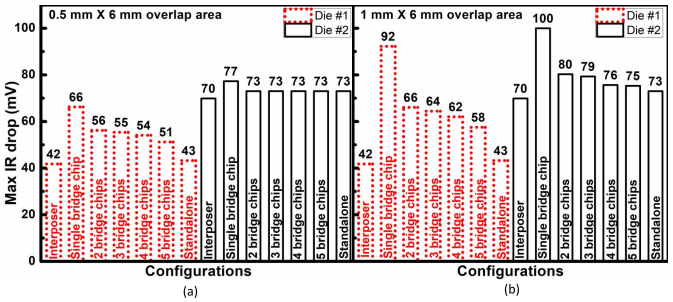


Fig. 4. IR-drop analysis results of (a) 0.5 mm × 6 mm overlap area, (b) 1 mm × 6 mm overlap area.

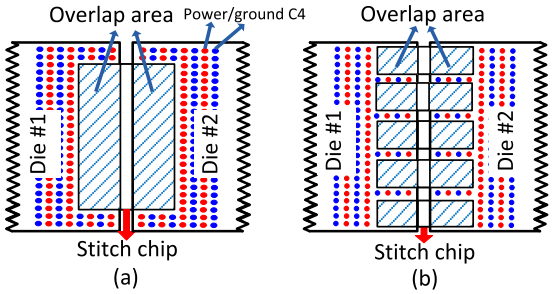


Fig. 5. Illustration of bridge-chip placement (a) a single large bridge-chip, (b) five small bridge-chips.

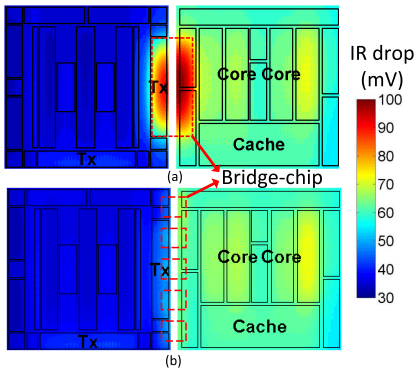
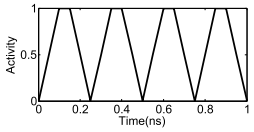


Fig. 6. The IR-drop profile of each die for (a) single large bridge-chip with a large overlap area of (1 mm × 6 *mm*), (b) 5 bridge chips with a small overlap area (0.5 *mm* × 6 *mm*).



(a)

Unit: mV	Die #1	Die #2
Standalone	103.19	160.46
Interposer	99.93	155.37
Bridge-chip (single)	132.29	170.80
Bridge-chip (five)	109.44	160.46

(b)

Fig. 7. (a) Current activity; (b) transient analysis results.

have an important impact on the PSN. Moreover, whether the interconnect bridging is comprised of a single large bridge-chip or several smaller bridge chips of the same aggregate area also impacts the maximum IR-drop. To investigate these effects, we consider two different overlap areas, and up to five bridge-chips, as shown in Fig. 5(a) and (b).

The results show that with smaller overlap area between the active dice and the bridge chips, we can minimize the IR-drop of the bridge-chip case the most. If we use five bridge-chips, instead of a single large bridge-chip, the maximum IR-drop has a nominal IR-drop increase and is comparable to the interposer case under consideration (4.1% larger). Fig. 6 shows the IR-drop noise profile of two evaluated bridge-chip cases. For the single bridge-chip case with larger overlap area, there are two noise hotspots at the edges of the two dice due to insufficient C4 power/ground bumps, as shown in Fig. 6(a). As a comparison, there are no clear noise hotspots on the edges if we utilize, for example, five bridge-chips with smaller overlap area, as shown in Fig. 6(b).

However, there is a trade-off between manufacturing complexity and power delivery noise mitigation by using multiple bridge-chips instead of a single large bridge-chip. For example, as bridge-chip count increases, so does the need for multiple high alignment accuracy assembly steps. Therefore, to reduce the assembly complexity, we prefer a smaller number of bridge chips. On the other hand, more bridge chips are preferred for reducing PSN. However in Fig. 4, we find that for both overlap areas considered, the PSN reduction rate in Die #2 begins to saturate when we use five bridge-chips and beyond which, there is a diminishing return as bridge-chip count increases.

2) Transient Droop: For transient analysis, we assume the chip current has a rise time, pulse time, fall time and period of 100 ps, 50 ps, 100 ps, and 250 ps, respectively. The current waveform is illustrated in Fig. 7(a). For the bridge-chip case, the overlap area is 0.5 mm × 6 mm.

The results are summarized in Fig. 7(b). Compared to the standalone case, the interposer achieves a PSN reduction of approximately 3.16% and 3.17% for Die #1 and Die #2, respectively. For the single bridge-chip case, the results are approximately 28.2% and 6.44% higher than the standalone case for Die #1 and Die #2, respectively. Likewise, we again find that the multiple bridge-chip configurations reduce the maximum switching noise. For the five bridge-chip case, there is only a 6.04% increase for Die #1 and a minimal increase for Die #2 because there are no noise hotspots in the peripherals of Die #2. Another observation is that the difference between the evaluated cases is not as significant as was in the IR-drop analysis since the switching noise mainly results from inductive parasitics in the package. Note, all PSN results in this letter are strongly dependent on the power-maps assumed; if a bridge-chip is within the footprint of a large power density region, PSN will be impacted more severely.

IV. Conclusion

This letter presents a PDN analysis framework for 2.5-D integrated platforms. The framework is used to benchmark interposer and bridge-chip based 2.5-D integration technologies. The use of dense power/ground grids in an interposer along with fine-pitch power/ground microbumps provides minimal improvement in PSN compared to the considered standalone case that uses a coarse power/ground C4 bumps. Moreover, in this letter, we discuss some design considerations in bridge-chip based interconnection platforms. Specifically, our results suggest that minimizing the bridge-chip-to-active die overlap regions suppresses PSN when there is no direct path for power delivery in the overlap regions. Using five bridge-chips with an overlap area of 0.5 × 6 *mm*, the bridge-chip based 2.5-D integration has comparable PSN to an interposer with dense power/ground grids and microbumps.

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